MAY.26.2005 10:54AM SYNOPSYS INC RECEIVED CENTRAL FAX CENTER NO.383 P.2/2

MAY 2 7 2005

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Appl. No.	:	09/760,063
Filed	:	01/12/01
Inventors	:	Kevin M. Harer, Pei-Hsin Ho and Robert F. Damiano
Title	:	SIMULATION-BASED FUNCTIONAL VERIFICATION OF MICROCIRCUIT DESIGNS

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

37 CFR 1.132 DECLARATION OF KEVIN M. HARER

I, Kevin M. Harer, being duly warned that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent resulting therefrom, declare that:

1. The term "Ho et al." shall be used in this Declaration to refer to the following publication: P. Ho, T. Shiple, K. Harer, J. Kukula, R. Damiano, V. Bertacco, J. Taylor and J. Long. Smart Simulation Using Collaborative Formal and Simulation Engines. In ICCAD, 2000, pp. 120-126.

2. To the extent Ho et al. discloses an invention or inventions claimed by the above-referenced patent application, Ho et al. is disclosing work that originated only from myself and my co-inventors as named in the above-referenced patent application.

3. In this Declaration, all statements made of my own knowledge are true, and all statements made on information and belief are believed to be true.

Dated: 05/26/05 (mm/dd/yy) By: Kevin M. Harer
Kevin M. Harer